WHAT IS CLAIMED IS:

1. A method of lowering bus power consumption on a transmitter and receiver pair, comprising the steps of:

receiving a first signal;

transmitting the first signal;

computing error calculation on the first signal; and

powering down the transmitter and receiver.

2. The method of claim 1 wherein the step of receiving a first signal further includes a step of sending the first signal to a data layer by a device.

3. The method of claim 2 further comprising the steps of:

setting bits turned off in the first signal to zeros; and

computing error calculation on the first signal.

4. The method of 3 wherein the step of transmitting the first signal further includes the step of assuming first signal bits turned off are zeros.

5. The method of claim 4 further comprising the step of comparing the received signal and the transmitted signal.

6. The method of claim 5 wherein the step of powering down the transmitter and receiver is based on the step of comparing.

7. The method of claim 1 further comprising the steps of:

receiving a second signal;

transmitting the second signal;

comparing the first signal with the second signal; and

powering up the transmitter and receiver.

8. The method of claim 7 wherein the step of receiving a second signal further includes a step of sending the second signal to a data layer by a device.

9. The method of claim 8 wherein the step of receiving a second signal further includes a step of changing pattern of the second signal bits left on.

10. The method of claim 9 wherein the step of comparing further includes comparing pattern of the bits left on from the first signal and the second signal.

11. The method of claim 10 wherein the step of powering up is based on the step of comparing the first signal to the second signal.

12. An apparatus comprising:

a first device sending a first signal;

a second device receiving the first signal, wherein the second device computes error calculation on the first signal and the apparatus powers down the first and second device based on the error calculation.

13. The apparatus of claim 12 further comprising a data layer, wherein the data layer receives the first signal and sends the first signal to the first device.

14. The apparatus of claim 13 wherein the first device sets bits turned off in the first signal to zeros and performs error calculation on the first signal.

15. The apparatus of claim 14 wherein the second device assumes the first signal bits turned off are zeros.

16. The apparatus of claim 15 wherein the receiver compares the first signal received from the transmitter and result of the error calculation on the first signal.

17. The apparatus of claim 16 further comprising the first device receiving a second signal, the first device sending the second signal to the second device, the second device compares the first and second signals and the first and second device power up.

18. The apparatus of claim 17 wherein the data layer receives the second signal and sends the second signal to the first device.

19. The apparatus of claim 18 wherein the first device changes pattern of the bits left on in the second signal.

20. The apparatus of claim 19 wherein the second device compares the pattern of the bits left on from the first signal and the second signal.